In response to the Final Office Action, kindly amend the above-identified application as follows.

AMENDMENTS

In the Claims

Please amend claims 1, 7, 10, 15, 20-21, and 26 as shown in the PENDING CLAIMS section that begins with page 3 of this paper. Please add new claims 27-36 as shown in the PENDING CLAIMS section. Claims 2-6, 8-9, 11-14, 16-19, and 22-25 remain unchanged from the previous amendment, which are also presented in the PENDING CLAIMS section so as to constitute the entire set of the pending claims. A marked-up version for the claims being changed by this amendment is attached herewith as separate sheets titled "Version with Markings to Show Changes Made."

PENDING CLAIMS

1. (Twice Amended) A Clock Data Model (CDM) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising:

partitioning a complete clock net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based at least on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form a complete clock net simulation; and

storing the plurality of simulations in the Clock Data Model, said storing including:

storing the simulated load for each point where the local clock net is connected to the global clock net.

2. (Unamended) The CDM as defined in claim 1, wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates.

3. (Unamended) The CDM as defined in claim 1, wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net.

4. (Unamended) The CDM as defined in claim 3, wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net.

5. (Unamended) The CDM as defined in claim 1, wherein at least two of the plurality of local clock nets are simulated in parallel.

6. (Unamended) The CDM as defined in claim 1, wherein simulating each of the plurality of local clock nets comprises:

extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

extracting component values of the elements of the local clock net from the microprocessor network database;

simulating the local clock net based on the layout and the component values; and

extracting a load of the local clock net on the global clock net.

7. (Twice Amended) The CDM as defined in claim 6, wherein said simulating the local clock net includes:

setting clock arrival times from the global clock net to be simultaneous at all points where a given local clock net is connected to the global clock net.

8. (Once Amended) The CDM as defined in claim 1, wherein simulating the global clock net comprises:

extracting the layout of the global clock net from a microprocessor network database;

extracting component values of the elements of the global clock net from the microprocessor network database;

extracting the simulated loads of the plurality of local clock nets from the CDM; and

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

9. (Once Amended) The CDM as defined in claim 1, wherein the method further comprises evaluating the complete clock net simulation to determine whether results of the simulations converge.

10. (Twice Amended) The CDM as defined in claim 9, wherein, if the results do not converge, the method further comprises:

setting clock arrival times to be those calculated for the simulated global clock net;

re-simulating the at least one of the plurality of local clock nets using the corresponding calculated clock arrival time, to generate a load for the at least one local clock net on the global clock net;

re-simulating the global clock net based at least on the simulated or re-simulated load of each of the plurality of local clock nets; and

combining the simulations and re-simulations to form the complete clock net simulation.

11. (Unamended) The CDM as defined in claim 10, wherein re-simulating at least one of the plurality of local clock nets comprises:

re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times; and

extracting a load of the at least one local clock net on the global clock net.

12. (Unamended) The CDM as defined in claim 11, wherein the method further comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net.

13. (Unamended) The CDM as defined in claim 10, wherein re-simulating the global clock net comprises:

inserting the simulated or re-simulated loads of the plurality of local clock nets; and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads.

14. (Unamended) The CDM as defined in claim 10, wherein the method further comprises storing the plurality of re-simulations in the Clock Data Model.

15. (Twice Amended) A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the system comprising means for partitioning a complete clock net into a global clock net and a plurality of local clock nets, means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, means for simulating the global clock net based at least on the simulated load of each of the plurality of local clock nets, and means for combining the plurality of simulations to form a complete clock net simulation, the CDM comprising:

means for storing the plurality of simulation results, said means for storing including:

means for storing the simulated load for each point where the local clock net is connected to the global clock net.

16. (Unamended) The CDM as defined in claim 15, further comprising means for collecting all of the information created during the plurality of simulations.

17. (Unamended) The CDM as defined in claim 15, further comprising means for retrieving all of the information created during the plurality of simulations.

18. (Unamended) The CDM as defined in claim 15, further comprising means for querying all of the information created during the plurality of simulations.

19. (Unamended) The CDM as defined in claim 15, further comprising a timing tool interface to provide accurate clock arrival times for each clocked element in the microprocessor design.

20. (Twice Amended) The CDM as defined in claim 15, wherein the system further comprises means for evaluating the complete clock net to determine whether the results converge, means for setting clock arrival times to be those calculated for the simulated global clock net, means for re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, means for re-simulating the global clock net based at least on the simulated or re-simulated load of each of the plurality of local clock nets, and means for combining the simulations and re-simulations to form the complete clock net simulation and wherein the CDM further comprises means for storing the plurality of re-simulation results.

21. (Twice Amended) A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the system comprising a partitioner for horizontally and vertically

partitioning a complete clock net into a global clock net and a plurality of local clock nets, at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, a global clock net simulator for simulating the global clock net based at least on the simulated load of each of the plurality of local clock nets, and a merging unit for combining the plurality of simulations to form a complete clock net simulation, the CDM comprising:

a memory for storing the plurality of simulation results.

22. (Unamended) The CDM as defined in claim 21, further comprising means for collecting all of the information created during the plurality of simulations.

23. (Unamended) The CDM as defined in claim 21, further comprising means for retrieving all of the information created during the plurality of simulations.

24. (Unamended) The CDM as defined in claim 21, further comprising means for querying all of the information created during the plurality of simulations.

25. (Unamended) The CDM as defined in claim 21, further comprising a timing tool interface to provide accurate clock arrival times for each clocked element in the microprocessor design.

26. (Twice Amended) The CDM as defined in claim 21, wherein the system further comprises a convergence evaluator for evaluating the complete clock net to determine whether the results converge and, when the results are found not to converge, the system sets clock arrival times to be those calculated for the simulated global clock net, the at least one local clock net simulator re-simulates at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, the global clock net simulator re-simulates the global clock net based at least on the simulated or re-simulated load of each of the plurality of local clock nets, and the merging unit combines the simulations and re-simulations to form the complete clock net simulation and wherein the CDM further comprises a memory for storing the plurality of re-simulation results.

27. (New) The CDM as defined in claim 1, wherein said storing the plurality of simulations further includes:

storing clock arrival time and slope for each point where the local clock net is connected to the global clock net.

28. (New) The CDM as defined in claim 27, wherein said storing the plurality of simulations further includes:

storing location of each point where the local clock net is connected to the global clock net.

29. (New) The CDM as defined in claim 1, wherein said storing the plurality of simulations further includes:

storing location of each point where a clocked element is connected to the local clock net.

30. (New) The CDM as defined in claim 29, wherein said storing the plurality of simulations further includes:

storing a name of the clocked element for each point where the clocked element is connected to the local clock net.

31. (New) The CDM as defined in claim 29, wherein said storing the plurality of simulations further includes:

storing clock arrival time and slope of the clocked element for each point where the clocked element is connected to the local clock net.

32. (New) The CDM as defined in claim 15, wherein said means for storing the plurality of simulations further includes:

means for storing clock arrival time and slope for each point where the local clock net is connected to the global clock net.

33. (New) The CDM as defined in claim 32, wherein said means for storing the plurality of simulations further includes:

means for storing location of each point where the local clock net is connected to the global clock net.

34. (New) The CDM as defined in claim 15, wherein said means for storing the plurality of simulations further includes:

means for storing location of each point where a clocked element is connected to the local clock net.

35. (New) The CDM as defined in claim 34, wherein said means for storing the plurality of simulations further includes:

means for storing a name of the clocked element for each point where the clocked element is connected to the local clock net.

36. (New) The CDM as defined in claim 34, wherein said means for storing the plurality of simulations further includes:

means for storing clock arrival time and slope for each point where the clocked element is connected to the local clock net.